Small Signal Response of Inversion Layers in High Mobility $In_{0.53}Ga_{0.47}As$ MOSFETs Made with Thin High-κ Dielectrics

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Ultra-high mobility compound semiconductor-based MOSFETs and quantum-well FETs could enable the next generation of logic transistors operating at low supply voltages since these materials exhibit excellent electron transport properties. While the long channel $In_{0.53}Ga_{0.47}As$ MOSFET characteristics exhibit promising characteristics with unpinned Fermi level at the InGaAs-dielectric interface, the high field channel mobility as well as sub-threshold characteristics needs further improvement. There could be contribution from one or several potential scattering processes to cause mobility degradation in surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs such as interface roughness, remote or local optical phonon scattering and remote Coulomb scattering due to charges in the gate oxide. In this work, we present a comprehensive equivalent circuit model that accurately models the experimental small signal response of inversion layers in $In_{0.53}Ga_{0.47}As$ MOSFETs fabricated with $LaAlO_3$ gate dielectric and enables accurate extraction of effective channel mobility. Temperature dependent measurements allow us to identity the various scattering mechanisms.

Introduction

Continued miniaturization of the silicon CMOS transistor technology, has resulted in an unprecedented increase in single-core and multi-core performance of modern-day microprocessors. However, the exponentially rising transistor count has also increased the overall power consumption, making performance per watt of energy consumption the key figure-of-merit for today's high-performance microprocessors. Today, energy efficiency serves as the central tenet of high performance microprocessor technology at the system architecture level as well as the transistor level ushering in the era of energy efficient nanoelectronics. Aggressive supply voltage scaling while maintaining the transistor performance is a direct approach towards reducing the energy consumption since it reduces the dynamic power quadratically and the leakage power linearly. To that effect, ultra-high mobility compound semiconductor-based (e.g. Indium antimonide, Indium arsenide and $In_xGa_{1-x}As$) MOSFETs and quantum-well FETs could enable the next generation of logic transistors operating at low supply voltages since these materials exhibit excellent low-field and high-field electron transport properties (1)-(3). Significant literature exists on the demonstration of $In_{0.53}Ga_{0.47}As$ based MOSFETs fabricated with various in-situ and ex-situ deposited high-k dielectrics. While the long channel $In_{0.53}Ga_{0.47}As$ MOSFET characteristics are promising exhibiting unpinned Fermi level at the $In_{0.53}Ga_{0.47}As$ -dielectric interface and high peak values of inversion channel mobility,

the high field channel mobility has been disappointingly low. There could be contribution from one or several potential scattering processes to cause mobility degradation such as interface roughness, remote soft optical phonon scattering, polar optical phonon scattering from $In_{0.53}Ga_{0.47}As$ itself and remote Coulomb scattering due to charges in the oxide and/or interface. Besides the mobility degradation, the accuracy of the mobility measurement in the weak and strong inversion regime using the conventional split C-V measurement technique is also of significant concern due to the high density of fast responding interface traps in the upper half of the $In_{0.53}Ga_{0.47}As$ band gap, tunneling gate leakage as well as distributed effects due to the channel resistance, particularly in long channel devices.

Effective channel mobility as a function of the transverse effective electric field or inversion carrier density is an important metric for characterizing the performance of $In_{0.53}Ga_{0.47}As$ based MOSFETs since it not only affects the long channel MOSFET performance directly but also determines indirectly the short channel MOSFET performance in the non ballistic regime by influencing the source side injection velocity (4). The split CV measurement of the MOSFET inversion capacitance is the standard technique of extracting the effective channel mobility of MOSFETs which involves direct estimation of the mobile inversion charge density (N_{inv}) through the gate to channel capacitance (C_{gc}) as a function of the gate to source voltage (V_g)

$$Q_{inv} = \int_{-\infty}^{Vg} C_{gc}(V)dV \qquad [1]$$

While this method is reliable and highly accurate for most Silicon based MOSFETs including the high-κ/metal-gate Si MOSFETs, it is less straight forward in the case of $In_{0.53}Ga_{0.47}As$ MOSFETs. In InGaAs-based MOSFETs, the complex nature of the semiconductor-dielectric interface with relatively high density of interface states, D_{it}, can exhibit a capacitance, C_{it} , that contributes significantly to the measured C_{gc}, even in inversion leading to an over estimation of extracted N_{inv}. This can lead to incorrect evaluation of the effective channel mobility. $In_{0.53}Ga_{0.47}As$ and high-κ dielectric interfaces are known to possess interface defects. Although the exact origin of the defects is still under debate there is evidence that compound semiconductors exhibit interface states that arise from the native defects, such as Ga or As dangling bonds as well as Ga–Ga or As–As like-atom bonds created by unwanted oxidation during the process of gate dielectric formation. It has been proposed that the As-As anti bonding states due to local excess arsenic created during the gate oxide deposition can lead to a distribution of states that extend into the conduction band (5),(6). The presence of interface states near the conduction band leads to fast trap response as the Fermi level approaches or enters the conduction band in the inversion regime. Many recent publications of III–V MOSFETs have reported split C-V measurements and the resultant mobilities calculated from those measurements (7)–(9). Frequency dispersion due to C_{it} as well as lumped or distributed resistance effects in the inversion regime has strongly influenced the C_{gc} vs V_g (or C-V) curves resulting in incorrect mobility calculations. Very recently, Hinkle et al reported on low temperature split C-V measurement at 77K to "freeze out" the D_{it} response in $In_{0.53}Ga_{0.47}As$ MOSFETs and claimed the 77K C-V data reflecting the true inversion capacitance (10). However, a close inspection of the 77K C-V data reveals persistent frequency dispersion, albeit low compared to 300K C-V data, in the inversion response of

the carriers. In this paper we will outline a novel technique that self consistently solves the capacitance-voltage (C-V) and conductance-voltage (G-V) measurement data as a function of gate bias and small signal AC frequency to uniquely determine the D_{it} response as well as the true inversion carrier response for a given voltage. This technique enables us to extract the true inversion capacitance (C_{inv}) as a function of temperature and gate bias in the inversion regime. The impact of parameters such as oxide capacitance, tunnel conductance, fixed series resistance, distributed channel resistance and interface state time constant on the extraction of the interface state density, its response time as well as the true inversion carrier density is systematically studied using the experimental data. Unlike previous work, this work does not assume any particular D_{it} distribution prior to performing the C-V and G-V fitting exercise and does not assume that a low temperature C-V data is necessarily free from D_{it} effect. Instead, the technique directly extracts the interface state density, trap time constant and the frequency independent inversion channel capacitance by directly solving an equivalent circuit model from the measured admittance values. As an example, Figures 1(a) and 1(b) highlight the dramatic effect of frequency dispersion in the split C-V on the extracted mobility and inversion carrier density. The figures also show for comparison the mobility and inversion carrier density corrected for the interface states, distributed channel resistance and gate leakage using the model described in this paper. Even though the inversion carrier density directly extracted from the uncorrected 1.6 MHz C-V curve at 77K is close to the true inversion carrier density at 77K, the low field peak mobility extracted is still significantly affected.

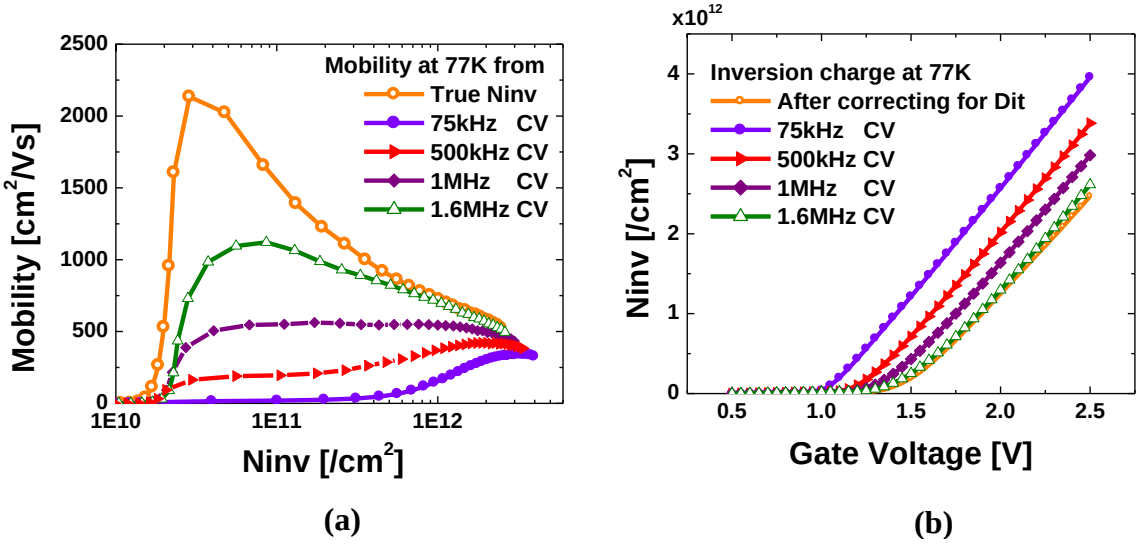


Figure 1 Comparison of (a) effective channel mobility and (b) inversion carrier density at 77K with and without correction for interface states, gate leakage and distributed channel resistance

Factors Affecting Split CV Measurements

In this section, we systematically explain the impact of distributed channel resistance, gate leakage and interface states on the admittance behavior of an $In_{0.53}Ga_{0.47}As$ MOS transistor biased in weak and strong inversion.

A. Effect of Distributed Channel Resistance

Since the interface states in the upper half of the semiconductor band gap can respond to small signal AC frequencies in the split capacitance measurement, one minimizes the error either a) by increasing the small-signal measurement frequency or b) by lowering the temperature of measurement so that the interface traps cannot follow the fast changing AC signal. However, the distributed nature of the channel resistance comes into play at higher frequencies which causes the measured capacitance to be lower than the true capacitance, resulting in an under-estimation of N_{inv}. This is illustrated in Figure 2(a) where the frequency dispersion in both C-V and G-V data is caused solely by the channel resistance. Physically, the distributed channel resistance accounts for the energy loss during the minority carrier transport between the source/drain at any given position in the channel. As the channel length increases the dispersion in C-V and G-V increases due to the increased channel resistance.

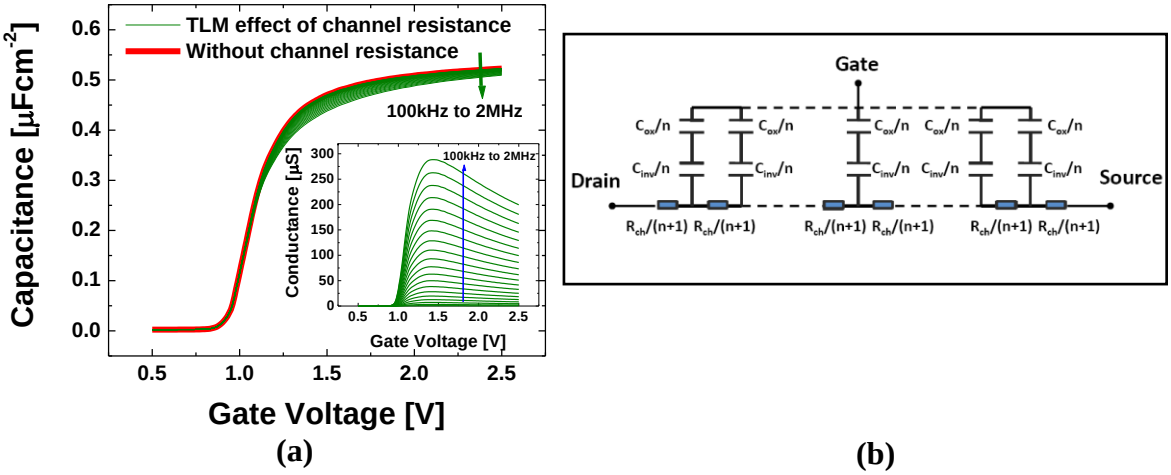


Figure 2 (a) Effect of distributed channel resistance on the measured C-V and G-V characteristics (b) Equivalent circuit of a MOSFET in inversion incorporating the channel resistance and ignoring the effects of interface states and gate leakage.

B. Effect of Gate Leakage

In the case of ultra thin gate dielectric with significant gate leakage, we need to consider the effect of the tunnel conductance that shunts the oxide capacitance as well as the interface state capacitance. A direct impact of this increased tunnel conductance which appears in series with the channel and series resistance is shown in Figure 3(a) where an increasing percentage of the AC test voltage appears across the channel resistance as gate leakage increases with higher V_g leading to a droop in the measured C-V characteristics. In the inset of Figure 3(a), we show the effect of increased tunnel conductance on the G-V data where there is a linear monotonic increase in the measured conductance as the gate voltage is increased.

C. Effect of Interface States

Here we analyze the effect of interface states on the split C-V characteristics. The frequency dispersion in the C-V data caused by the D_{it} effect is shown in Figure 5a). An

arbitrary linear D_{it} distribution across the upper half of the bandgap is assumed as an illustrative example in this case to calculate the frequency dispersion in the C-V and G-V as shown in the inset of Figure 4a. The presence of D_{it} causes a frequency dependent "threshold voltage shift" in the C-V characteristics. At lower frequencies, the capacitance rises at lower V_g due to strong contribution from the midgap states, while at higher frequencies the midgap states cannot respond and the contribution comes primarily from the band edge states which are active at higher V_g. The conductance peak will also shift to higher Vg's with higher frequencies as the band edge states get activated.

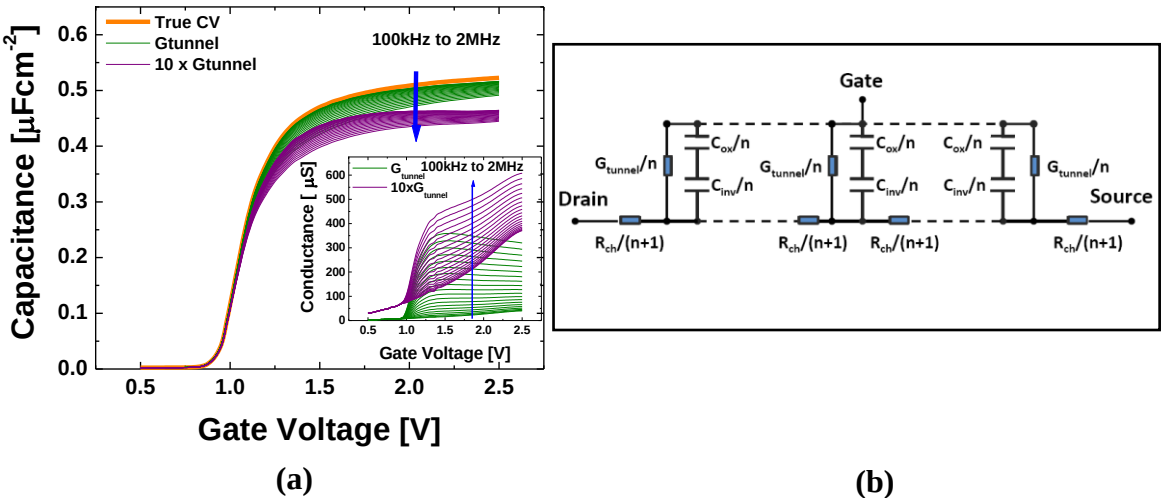


Figure 3 (a) Effect of tunnel conductance due to gate to channel leakage on the measured C-V and G-V characteristics (b) Equivalent circuit of a MOSFET in inversion incorporating the tunnel conductance, the distributed channel resistance and the contact resistance at each end of the channel.

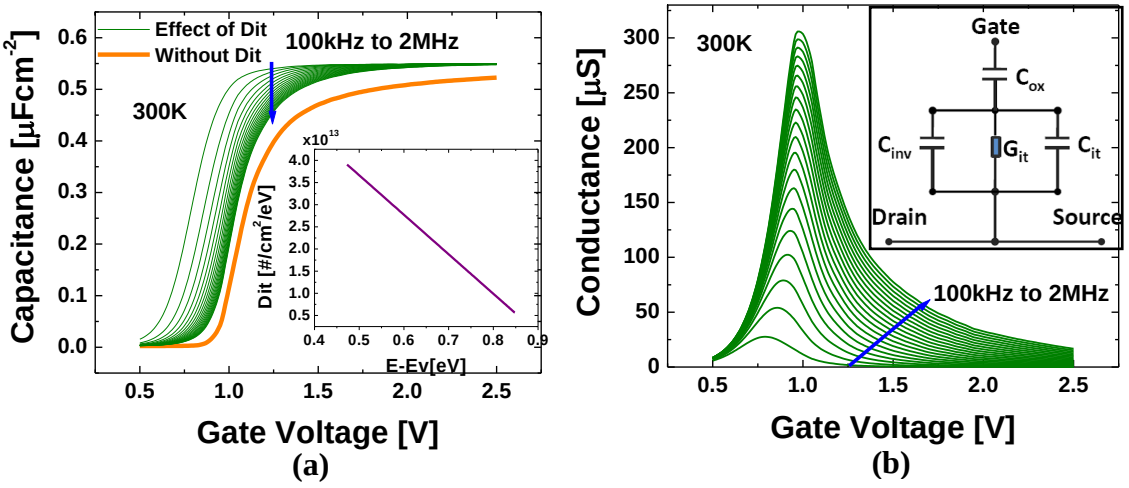
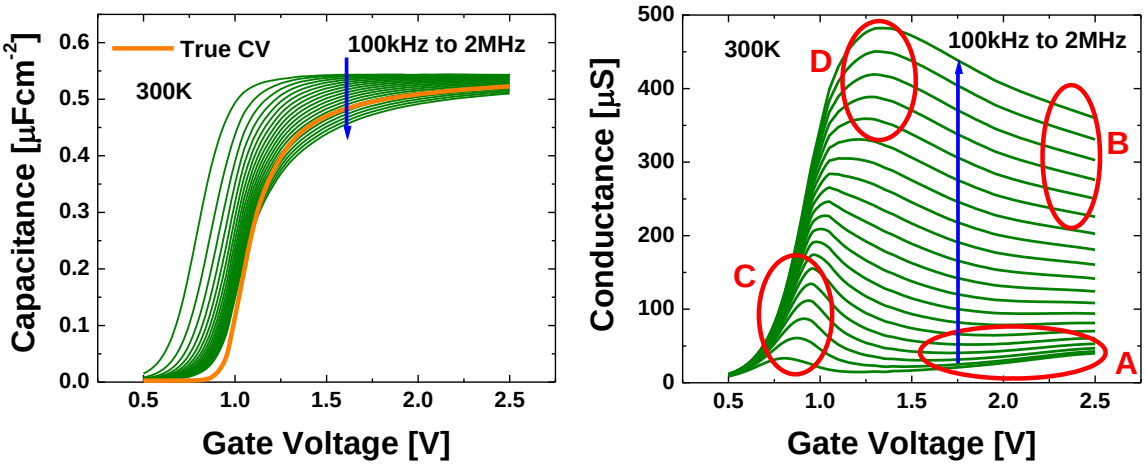


Figure 4 (a) Effect of interface states, Dit, on the measured C-V characteristics (b) Effect of interface states, Dit, on the measured G-V characteristics. The equivalent circuit model in inversion incorporating the effect of Dit is shown in the inset of (b)

D. Effect of Channel Resistance, Gate Leakage and Interface States

Finally, we show the combined effects of series contact resistance, distributed channel resistance, gate leakage and interface states on the C-V and G-V characteristics in the inversion regime in Figures 5(a) and (b). We identify the various regimes marked as A, B, C and D in the G-V-f characteristics. In region A, at high gate voltage and low frequency, the measured conductance values are directly related to the tunneling conductance estimated from the DC gate leakage measurements. In region B, at high gate voltage and high frequency the series resistance (from contact resistance and distributed channel resistance) effect markedly increases the frequency dispersion of the measured conductance. It should be noted that in the high gate voltage regime as the Fermi level sits deep inside the conduction band the interface state conductance is negligible and the measured conductance is only the tunneling conductance modified by the series resistance and the measurement frequency. In region C, at lower gate voltage and lower frequency, the conductance peak exhibits strong frequency dependence due to contribution from the near midgap states. In region D, at intermediate gate voltage and higher measurement frequency the conductance contribution comes from the band edge states. The equivalent circuit model is described comprehensively in the next section.



(a) **(b)**

Figure 5 Effect of interface states, series resistance (contact and channel) and tunnel conductance on the (a) measured C-V characteristics and (b) measured G-V characteristics.

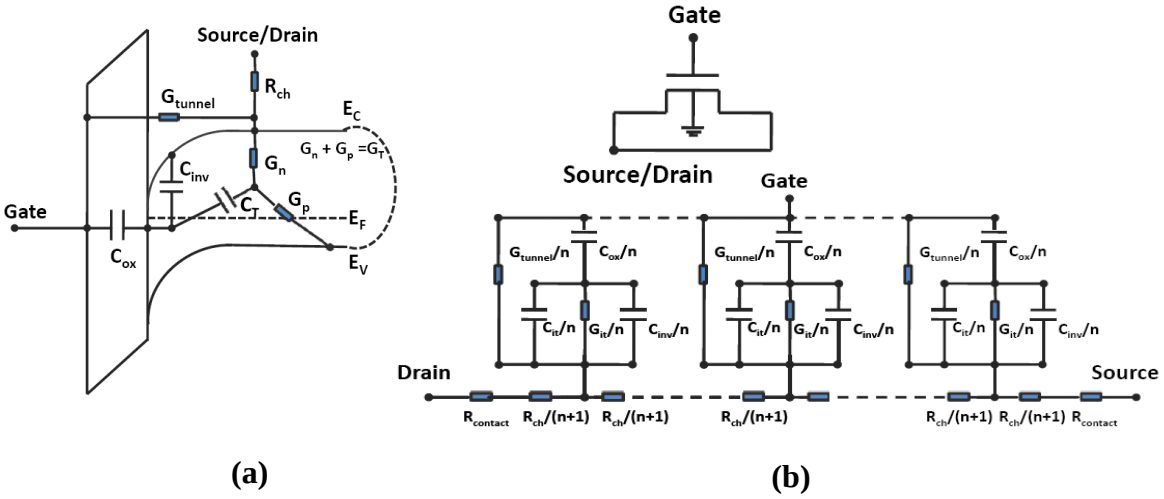
Device Fabrication

The samples consisting of a 150 nm thick carbon-doped ($2x10^{18}$ cm^{-3}) $In_{0.52}Al_{0.48}As$ buffer layer followed by an 80 nm thick $In_{0.53}Ga_{0.47}As$ layer doped with $3x10^{17}$ carbon/cm^{-3} were grown on heavily doped p-type InP substrate using a conventional effusion-source molecular beam epitaxy (MBE) reactor equipped with an As cracker producing As_2 flux. An amorphous 0.5 nm thick Si layer was grown at ~100 ^{o}C for *in-situ* passivation followed by capping with 20 nm arsenic at 20 ^{o}C. The purpose of As_2 capping was to prevent the surface oxidation while transferring the wafers to another MBE system for $LaAlO_3$ deposition. The arsenic cap was thermally desorbed in ultra high vacuum at

300 ^{o}C, and amorphous $LaAlO_3$ layer of 20 nm was deposited by MBD at ~100 ^{o}C in molecular oxygen at a background pressure of 2×10^{-6} Torr, followed by *in- situ* annealing at ~340 °C in a mixture of molecular oxygen and ozone (~10%) at the same background pressure. 200 nm thick TaN metal gate deposited *ex-situ* by the physical vapor deposition (PVD) serves as gate electrode. Self-aligned MOSFETs were fabricated by implanting Si^{+} ions (dose - 5×10^{14} cm^{-2}, energy – 50 keV) into source and drain regions followed by rapid thermal anneal at 750^{o}C for 15 sec. The source and drain regions were separated using ring-like gate configuration with the channel length of 3 µm to 50 µm and length-to-width (L/W) ratio of ~140 to ~ 10, respectively. $LaAlO_3$ was effectively removed using combination of RIE and HCl etching, and the S/D contacts were made by electron beam evaporation of PdGe followed by annealing at 400^{o}C for 20 sec.

The Equivalent Small Signal Model

A standard LCR meter (HP4285A) was used to measure the capacitance (Split C-V) and conductance as a function of frequency and voltage for a range of temperature from 300K till 25K. Measurements were made in parallel mode with a small signal AC amplitude of 25 mV. The equivalent model in inversion including all the effects described in previous section is shown in Figures 6(a)-(b).



(a) **(b)**

Figure 6 a) Equivalent circuit for an n-channel MOSFET in inversion (b) Distributed equivalent circuit model in weak and strong inversion: C_{ox} = oxide capacitance, G_{tunnel} =tunnel conductance, C_{it} = interface trap capacitance, G_{it} = interface trap conductance, C_{inv} = semiconductor inversion capacitance, R_{ch} = the gate bias dependent inversion channel resistance, $R_{contact}$ = series resistance associated with implanted source/drain regions, contacts and metal pads.

The model incorporates several features which are currently absent in the recent publications, while extracting the true N_{inv} and D_{it}, especially when the channel is close to inversion or inverted. For example, the first steps in the formulation of the model are the inclusion of the fixed series resistance, $R_{contact}$, at the two ends of the channel. Also, due to the distributed nature of the inversion channel resistance, R_{ch}, we create a transmission line model (TLM) to accurately reflect the effect of R_{ch} as well as the tunnel conductance of the oxide, G_{tunnel}, arising from gate leakage. The gate oxide or insulator capacitance, C_{ox}, is estimated from the maximum capacitance measured in accumulation. We verify

the validity of our C_{ox} estimation by comparing with physical measurements (cross section TEM) as well as from minimizing the error between the calculated and measured C-V / G-V data points across the frequency range during the extraction process. A closed form equation was derived to model the admittance of the circuit shown in Figure 6(b).

The measured admittance between the gate and source/drain for the circuit shown in Figure 6(b) is given by equation [2],

$$Y_m = G_m + j\omega C_m \qquad [2]$$

where G_m and C_m are the measured conductance and capacitance respectively. C_m and G_m are given by equations [3] and [4],

$$C_m = \mathrm{Re}\left[\frac{C'\tanh(\lambda)}{\lambda}\right] + \frac{G_{it}}{C_I\omega}\mathrm{Im}\left[\frac{C'\tanh(\lambda)}{\lambda}\right] + \frac{G_{tunnel}}{\omega}\mathrm{Im}\left[\frac{\tanh(\lambda)}{\lambda}\right] \quad [F/cm^2] \quad [3]$$

$$\frac{G_m}{\omega} = -\mathrm{Im}\left[\frac{C'\tanh(\lambda)}{\lambda}\right] + \frac{G_{it}}{C_I\omega}\mathrm{Re}\left[\frac{C'\tanh(\lambda)}{\lambda}\right] + \frac{G_{tunnel}}{\omega}\mathrm{Re}\left[\frac{\tanh(\lambda)}{\lambda}\right] \quad [F/cm^2] \quad [4]$$

where λ is $\frac{\gamma L}{2}$, and γ, C', C_I and G_{tunnel} are given by equations [5] – [8] respectively.

$$\gamma^2 = r_1\left[j\omega C' + \frac{C'}{C_I}G_{it} + G_{tunnel}\right] \qquad [5]$$

$$C' = \left[\frac{C_{ox}C_I}{C_{ox} + C_I + G_{it}/j\omega}\right] \qquad [6]$$

$$C_I = C_{inv} + C_{it} \quad [F/cm^2] \qquad [7]$$

$$G_{tunnel} = \frac{1}{WL}\frac{\Delta I_g}{\Delta V_g} \quad [S/cm^2] \qquad [8]$$

Here C_{ox} is the oxide capacitance in F/cm^2 and $r_1 = \frac{1}{g_{ds}}\frac{W}{L}$ [Ω] . The admittance due to a distribution of interface traps is given by the capacitance, C_{it}, and the conductance, G_{it}, given by equations [9] and [10] respectively (11).

$$C_{it} = q\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau}\tan^{-1}(\omega\tau)P(\sigma_s, E)\,dE \quad [F/cm^2] \qquad [9]$$

$$\frac{G_{it}}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau}\ln\left(1+\omega^2\tau^2\right)P(\sigma_s, E)dE \quad [F/cm^2] \qquad [10]$$

A random spatial distribution of interface defects causes a spatial distribution in the band bending which is accounted by the integrand in equations [9] and [10] where, τ is the interface trap time constant, σ_s is the surface potential fluctuation and P is a Gaussian distribution with variance of σ_s^2.

The flowchart of the algorithm used to extract the interface states and the true mobile inversion charge using this solution is illustrated in Figure 7. The effect of surface potential fluctuation was not considered in our analysis of C_{it} and G_{it}. The TLM model was solved for τ, D_{it} and C_{inv} as explained in the algorithm. Figures 8(a) and (b) show the 300K experimental C-V and G-V data compared to the solution obtained from our model which shows excellent agreement.

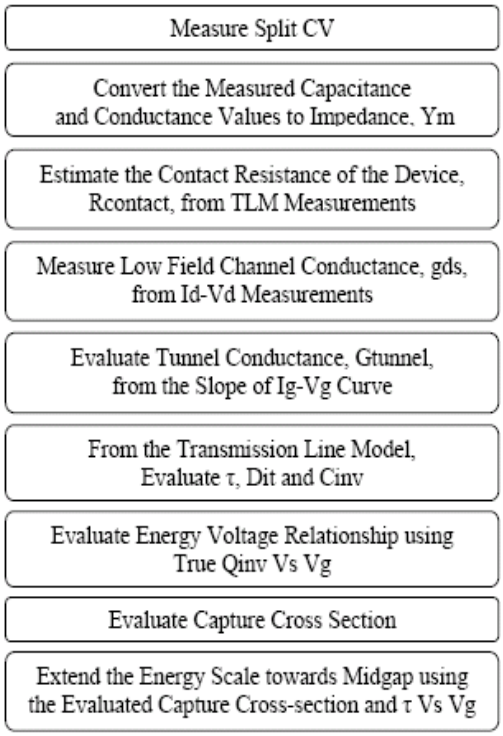


Figure 7 Flow chart of the algorithm used to extract the τ_{it}, D_{it} and N_{inv} from the measured CV and GV data in a self consistent fashion.

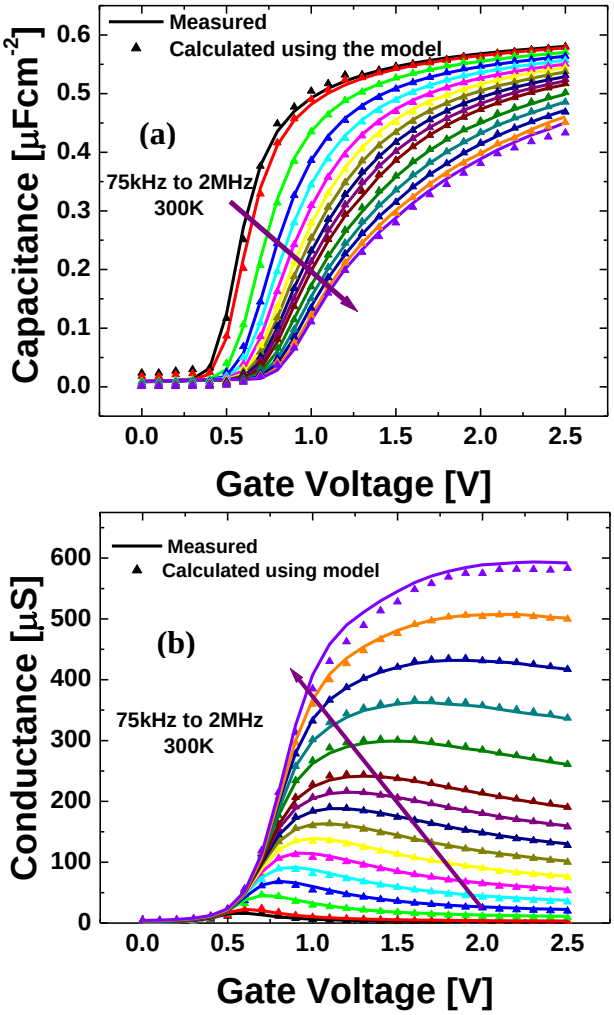


Figure 8(a) Experimental CV and (b) Experimental GV compared to solution from the split CV model

Extracting the D_{it}, τ and True N_{inv}

Having confirmed the validity of the proposed equivalent circuit, we proceed to extract the interface state density, its response time and the true inversion carrier density as a function of gate voltage. The key difference in our proposed method from the commonly used full conductance technique is that, *we do not need information about the peak position in the measured conductance (G_{it}/ω) versus frequency; we rather solve the conductance and the capacitance contribution of D_{it} in a self consistent manner over the entire frequency and voltage range.* This allows us to extract the D_{it} distribution over a wider energy distribution than given by the peak conductance method (12) for a given frequency range of the impedance measuring instrument at a given temperature. This also leads to an extraction of the true C_{inv} free from any frequency dispersion. We apply our technique to a wide range of operating temperatures of the $In_{0.53}Ga_{0.47}As$ MOSFET to extract the D_{it}, τ and true N_{inv} from 300K down to 25K.

The extracted D_{it} and τ are shown in Figures 9(a) and 9(b). It is noteworthy that the D_{it} profile extracted independently from the measured C-V and G-V data at 3 different temperatures are consistent with each other. Unlike the full conductance method, we can quantitatively extract the D_{it} over a wide range of energy at room temperature even though the precise location of the conductance peak, $(G_{it}/\omega)_{peak}$, is outside the measurement frequency range. In Figure 9(b), we compare the extracted time constant with the theoretical value calculated using the expression $\tau_e = \left(N_c \sigma v_t\right)^{-1} \exp(\Delta E / kT)$, where N_c is the effective conduction band density of states, σ is the capture cross section, v_t is the thermal velocity of electrons and $\Delta E = E_c - E$ is the energetic location of the trap with respect to the conduction band. Since we are analyzing the device in inversion we only need to account for the exchange of carriers with the minority band (i.e. conduction band for the p-type substrate). We get a strong agreement between the measured time constant and its theoretical estimate over a large range of energy and temperature, further validating our extraction approach.

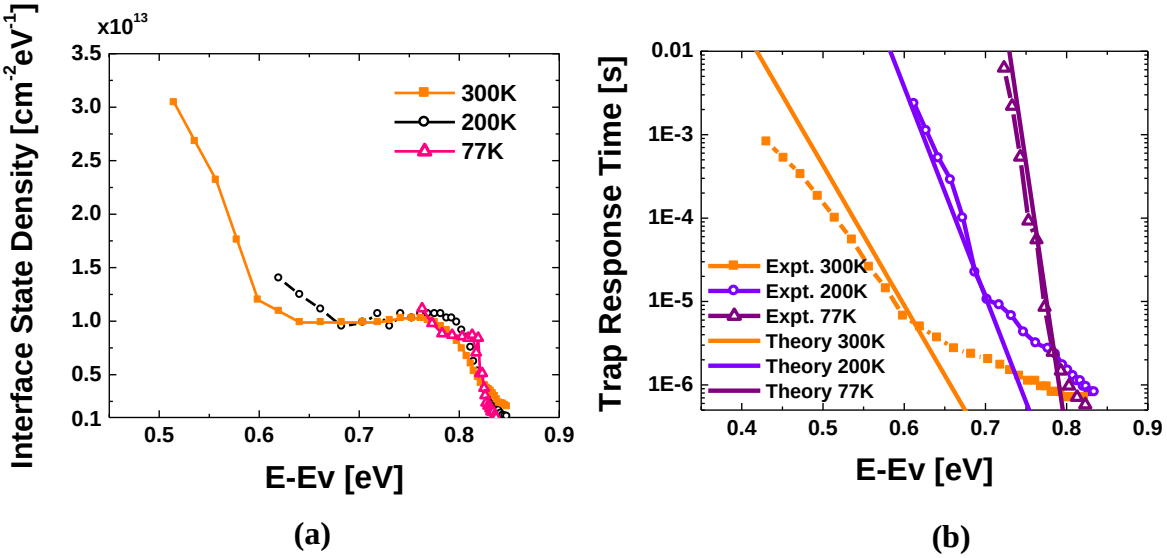


Figure 9 (a) Extracted interface state density versus energy (b) Extracted trap response time versus energy compared to theoretical response time.

Figures 10 (a-c) show the measured C-V characteristics exhibiting the effects described above and the extracted true inversion capacitance characteristics for 3 different temperatures. The true mobile inversion charge density as a function of Vg is plotted in Figure 11(a). The slope of each of the curves is roughly equal to 0.49 μF/cm^2 which is equivalent to the series combination of the $In_{0.53}Ga_{0.47}As$ inversion channel capacitance limited by density of states and the insulator capacitance, 0.65 μF/cm^2. The channel conductance data directly from the DC measurements at various temperatures are also shown in Figure 11(b).

The effective mobility as a function of the inversion carrier density can be directly extracted now from Figures 11(a) and (b) according to the following equation.

$$\mu = \frac{L}{W}\frac{g_{ds}}{Q_{inv}} \ [\mathrm{cm^2V^{-1}s^{-1}}] \qquad [11]$$

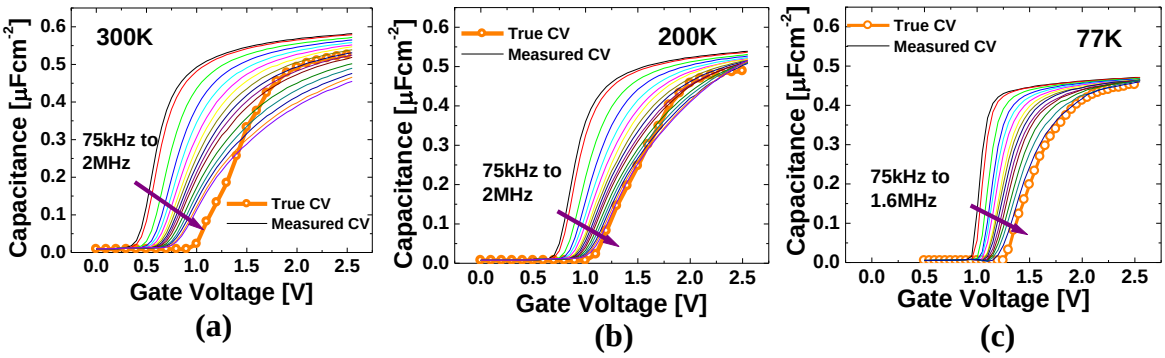


Figure 10 Measured C-V and extracted true C-V characteristics from $In_{0.53}Ga_{0.47}As$ MOSFETs at (a) 300K (b) 200K and (c) 77K

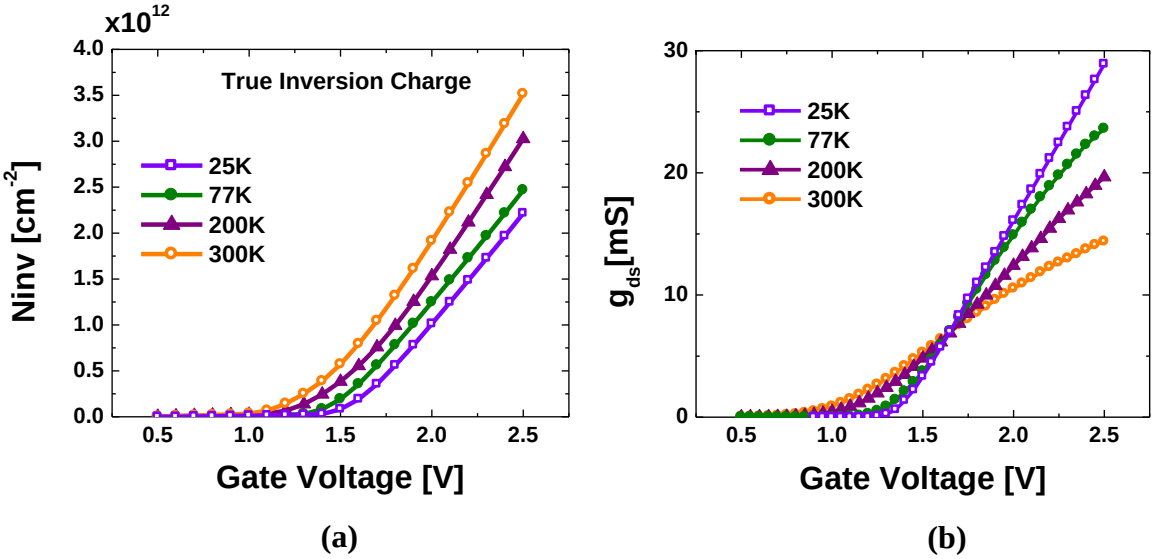


Figure 11 (a) Extracted N_{inv} from the C-V and G-V measurements and (b) the measured DC channel conductance data at 300K, 200K and 77K

The effective inversion channel mobility of $In_{0.53}Ga_{0.47}As$ MOSFETs is shown in Figure 12(a) as a function of temperature. At low N_{inv}, the mobility is dominated by Coulomb scattering while at higher N_{inv}, the mobility is dominated by phonon scattering mechanism as indicated by the temperature dependence shown in Figure 12(b). To understand and partition the various scattering components contributing to the total mobility we fit the measured data using the following model (13):

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{Phonon}} \qquad [12]$$

where, $\frac{1}{\mu_C} = \frac{\alpha T}{N_{inv}^{\ 2}}$, $\frac{1}{\mu_{Phonon}} = \frac{T}{\beta N_{inv}^{-0.3}}$ and $\frac{1}{\mu_{SR}} = \frac{1}{\gamma N_{inv}^{-2}}$.

We see acceptable agreement between the measured and the effective mobility model across a wide range of temperature and N_{inv}. As seen in Figure 13, at low N_{inv} the Coulomb scattering dominates and the mobility increases with higher inversion carrier density due to the screening effect. The Coulomb scattering at low inversion charge could be attributed to the net positively charged donor states present at the interface between the $In_{0.53}Ga_{0.47}As$ channel and the high-κ $LaAlO_3$ dielectric. The phonon limited mobility, μ_{Phonon}, dominates across a wide range of carrier density and has T^{-1} dependence. We attribute this to the soft polar optical phonon scattering as indicated by the weak temperature dependence. The phonons could originate remotely from the high-κ dielectric or could be associated with the polar nature of the InGaAs semiconductor or an interaction between the two.

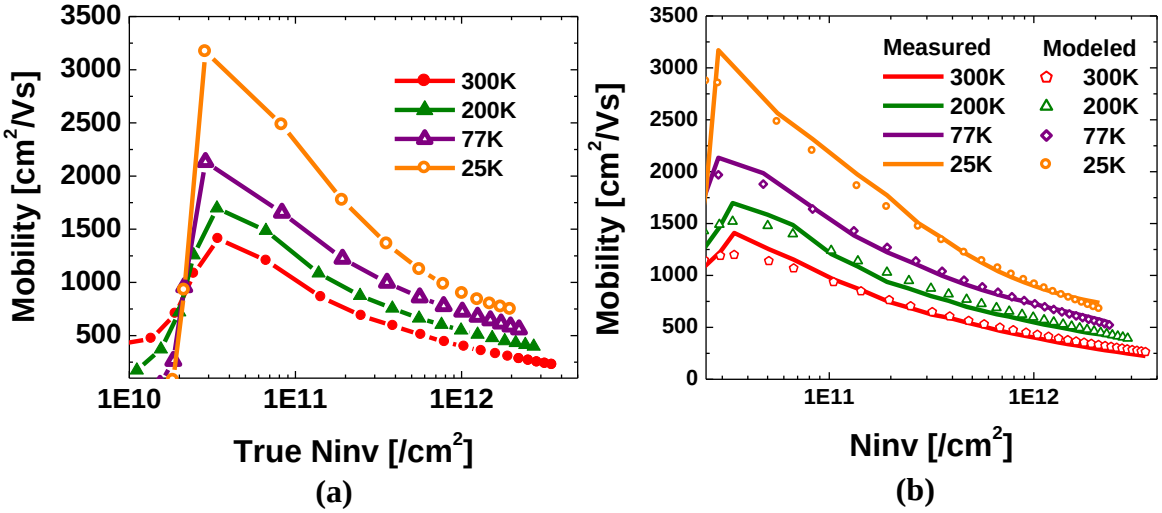


Figure 12(a) Effective mobility as a function of inversion charge (b) Experimental mobility compared with the model

In summary, we have presented here a comprehensive equivalent circuit model to analyze the true small signal response of inversion carriers in $In_{0.53}Ga_{0.47}As$ MOSFETs with high-k gate dielectric. Our approach attributes the frequency dispersion commonly observed in the C-V and the G-V measurement data of $In_{0.53}Ga_{0.47}As$ MOSFETs quantitatively to various contributing factors such as the interface states, contact

resistance, distributed channel resistance and the tunnel conductance. This allows us to self consistently solve for the frequency dependent interface state response and the frequency independent true inversion carrier density across a range of gate bias. The extraction methodology was validated across a broad temperature range which in turn enabled us to extract a temperature dependent time constant of interface traps as well as temperature dependent effective mobility to identity the scattering mechanisms.

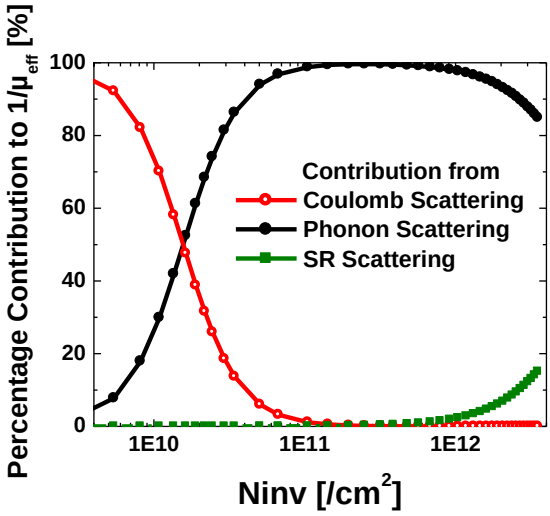


Figure 13 Percentage contributions of Coulomb, Phonon and Surface Roughness (SR) scattering to $1/\mu_{eff}$

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References

1. R. Chau, B. Doyle, S. Datta, K. Kavalieros and K. Zhang, *Nature Materials*, vol 6, pp. 810-812 (2007).
2. S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, et. al. , *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 685 (2007).
3. A. Ali et. al., Device Research Conference (2009).
4. J. Rhew, M. Lundstrom, *J. Appl. Phys.*, vol. 92, no. 9 (2002)
5. J. Robertson, *Journal of Microelectronic Engineering*, vol 86, pp 1558–1560 (2009).
6. E.P. O'Reilly, J. Robertson, *Phys. Rev. B* 34 (1984) 8684
7. Y. Xuan, P. D. Ye, and T. Shen, *Appl. Phys. Lett*. 91, 232107 (2007).
8. S. Koveshnikov, N. Goel, P. Majhi, C. K. Gaspe et. al., *66th Device Research Conf. Digest*, pp 43-44 (2008).
9. S. Koveshnikov, S. Oktyabrsky, D. Schlom, V. Tokranov et. al. *Appl. Phys. Lett. 93* (2008).
10. C. Hinkle et. al., *IEEE Electron Device Letters*, vol. 30, no. 4, pp. 316 (2009).
11. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, New York: Wiley, 1982.

12. K. Martens et. al., *IEEE Trans. Electron Dev*. 55, pp. 547–556 (2008).
13. O. Weber et. al., *Solid-State Electronics,* 50 626–631(2006).